LARGE-SIGNAL CHARACTERIZATION OF TWO-PORT NONLINEAR ACTIVE NETWORKS

by
Daniel C. Yang
and
D. F. Peterson
Electron Physics Laboratory
The University of Michigan
Ann Arbor, Michigan, 48104

ABSTRACT

A large-signal measurement technique for characterizing the single frequency behavior of nonlinear two-port networks is presented. Nonlinear networks are measured under various terminal conditions to establish optimal circuit design criteria. Results for common drain oscillator circuits are given as an example.

I. INTRODUCTION

Optimum performance of microwave solid-state components is achieved by establishing proper boundary conditions for the device in the form of an embedding network and excitation. Device characterization is a means of identifying these boundary conditions, by measurement, so that optimal circuits can be designed. The characterization of nonlinear devices is particularly difficult since the absence of the linear property generally precludes the determination of simple relationships among device terminal quantities.

In this paper, a new approach for characterizing the steady-state behavior of nonlinear active two-port networks is presented. This technique is primarily useful for optimizing the performance of single frequency amplifiers and oscillators. It is similar to the "two signal" method of [1], but provides more useful design information. Examples of this technique applied to an FET oscillator configuration and the resulting circuit design implications for VCO applications are presented.

II. CHARACTERIZATION APPROACH

Consider a nonlinear two-port network excited at each port by single-frequency, coherent incident power wave amplitudes a_1 and a_2 as shown in Fig. 1. At the fundamental frequency, reflected wave amplitudes b_1 and b_2 will exist and will depend on a_1 and a_2 as

$$b_1 = f_{b_1}(|a_1|, |a_2|, \varphi) \tag{1a}$$

$$b_2 = f_{b_2}(|a_1|, |a_2|, \varphi) \tag{1b}$$

where φ is the phase difference between a_1 and a_2. Reflected waves at higher harmonic frequencies are not considered in this technique. By adjusting $|a_1|, |a_2|$ and φ, the terminal conditions at each port are varied and optimal conditions (in some sense) can be identified. Such identification requires examination of the quantities b_1, b_2, a_1 and a_2, or some combination thereof. The measurement technique given here accomplishes this in a straightforward manner.

Reflection coefficients Γ_1 and Γ_2 can be defined as

$$\Gamma_1 = \frac{b_1}{a_1} = \gamma_1(|a_1|, |a_2|, \varphi) \tag{2a}$$

$$\Gamma_2 = \frac{b_2}{a_2} = \gamma_2(|a_1|, |a_2|, \varphi) \tag{2b}$$

so that the "state" of the network can be characterized by the set $\{\Gamma_1, \Gamma_2, |a_1|, |a_2|, \varphi\}$. Knowledge of φ is not particularly valuable, unless feedback is to be used around the network, and the two reflection coefficients and incident wave levels suffice to describe the state of the network. Γ_1 and Γ_2 ***should not*** be thought of as "input" or "output" reflection coefficients, but simply as the ratio of the terminal wave amplitudes.

A measurement system for providing $\Gamma_1, \Gamma_2, |a_1|, |a_2|$ is shown in Fig. 2. It simultaneously uses two network analyzer reflectometers to display Γ_1 and Γ_2 (or their reciprocals) and monitors $|a_1|^2$ and $|a_2|^2$ (incident power levels at each port). These two power levels can be independently adjusted and the phase difference is varied using a phase shifter in one arm.

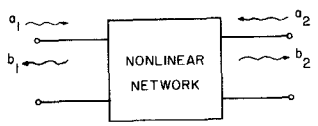

Fig. 1. Two-signal characterization of a non-linear two-port network.

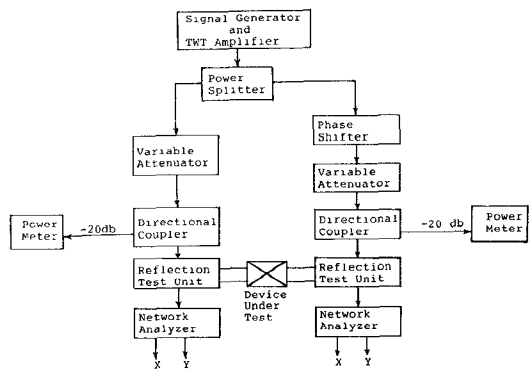

Fig. 2. Block diagram of the two-port large-signal measurement system.

0149-645X/82/0000-0345 $00.75

Each analyzer can be accurately calibrated in the usual way, and a calculator is used to collect, process, and store the measured results.

Useful interpretations of Γ_1 and Γ_2 are possible depending on the application of the two-port network. There are two important cases; amplifier operation and oscillator operation. These can be distinguished by considering the power crossing each port of the network, i.e.,

$$P_1=(|\Gamma_1|^2-1)|a_1|^2 \tag{3a}$$

$$P_2=(|\Gamma_2|^2-1)|a_2|^2 \tag{3b}$$

where positive P_1 or P_2 represents net power out of the associated port. For an amplifier, $|\Gamma_1|<1, P_1<0$ and $|\Gamma_2|>1, P_2>0$, i.e., power flows into port 1 (the "input") and out of port 2 (the "output"). The circuit boundary conditions would then be as shown in Fig. 3a, with a passive load of reflection coefficient $1/\Gamma_2$, and a source conjugate matched to Γ_1 for optimum power transfer. In the characterization, the harmonic converter associated with port 2 could be inverted to display $1/\Gamma_2$ or the required load impedance directly. By adjusting $|a_1|, |a_2|$, and φ in the system, the terminal conditions for maximum added power, maximum gain at a given power output, etc., can be determined.

In the case of an oscillator, $|\Gamma_1|>1$, $|\Gamma_2|>1$ and $P_1>0, P_2>0$, i.e., net power flows out of each port. The circuit boundary conditions necessary would then be as shown in Fig. 3b, with passive loads of $1/\Gamma_1$ and $1/\Gamma_2$ on ports 1 and 2 respectively. In the oscillator characterization, both harmonic converters can be inverted to directly display the terminations required. Again, the independent variables would be adjusted to maximize P_1 or P_2 or $P_1 + P_2$, etc., depending on the use of the oscillator. Only those conditions which allow $|\Gamma_1|>1$ and $|\Gamma_2|>1$ can be considered for oscillator operation.

III. APPLICATION TO FET OSCILLATORS

While optimization of FET or BJT power amplifiers is an important application of this characterization technique, the evaluation of FET oscillator performance and circuit specification is perhaps more interesting. A useful FET configuration for oscillators and VCOs in particular is the common drain arrangement. In this configuration, tuning can be accomplished at one port (the gate side) with low loss circuitry, while power is extracted at the other port (the source side) into a reasonable impedance level. Optimum terminations for the gate and source ports for VCO or single frequency oscillators can be found using the measurement technique described.

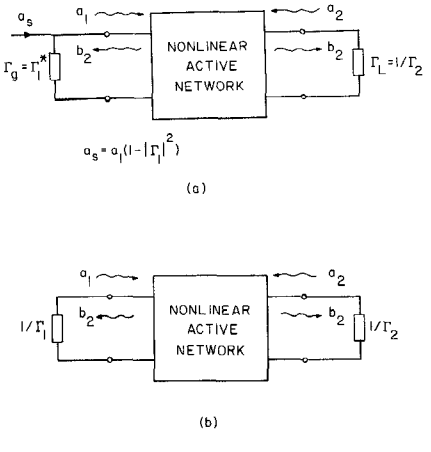

Fig. 3. (a) Circuit boundary conditions and excitation for amplifier operation, (b) circuit conditions for oscillator operation.

A 250 mW flip-chip FET was mounted in a symmetrical test fixture compatible with the measurement system. The coupling networks from the device terminals to the measurement reference planes were predetermined using an unterminating technique [2]. Hence, measured data could be easily transformed to the device terminals. The FET was biased in the common drain configuration, and a large amount of data was collected at various frequencies in the active mode when $|\Gamma_1|>1$ and $|\Gamma_2|>1$. The data was then interpreted for oscillator optimization.

Shown in Table 1 is the total output power $P_1 + P_2$ and corresponding terminating impedances at 7 GHz. The highest total power occurs for a lossless gate termination, and essentially all the power is available in the source load. As the loss in the gate termination increases, the total power drops, with more of it dissipated in the gate load. At high enough gate loss the total power becomes dominated by gate power, and the source power drops substantially with a corresponding large change in source load impedance. Shown in Fig. 4 are the gate and source load impedance regions corresponding to either highest source power or highest gate power. These data indicate the oscillator is optimized by using a low loss gate termination of prescribed reactance impedance level.

Shown in Table 2 is the optimum source load and maximum source power at 7 GHz as a function of the optimum gate load with increasing levels of gate loss resistance (i.e., tuning circuit loss). Hence for a varactor tuning circuit on the gate, the power output of the source and corresponding source load impedance can be specified for any given varactor series resistance. As indicated, for a series resistance of about 3 ohms, the maximum power from the source ha been halved to about 130 mW.

This FET configuration is useful for VCO applications since low-loss varactor tuning circuitry can be used at the gate. For a given level of varactor series resistance (gate loss), the available source power, optimum source load, and optimum gate reactance as a function of frequency can be determined, leading to optimum VCO design. Shown in Fig. 5 is the optimum source load impedance and corresponding power output versus frequency for a 4-ohm level of gate resistance (varactor series resistance). The points along the 4-ohm contour indicate the optimum gate reactance necessary

TABLE 1
Gate and source loading conditions for maximum total output power.

ReZs	ImZs	Ps(mW)	ReZg	ImZg	Pg(mW)	Ptot(mW)
74.74	43.52	265.99	0.46	63.53	3.24	269.24
77.31	43.24	241.37	0.73	63.42	5.16	246.53
73.11	47.63	237.75	0.30	64.98	1.78	239.52
81.97	42.79	203.22	1.27	63.44	9.15	212.37
85.66	38.80	192.12	1.55	62.09	13.15	205.27
85.68	38.77	192.04	1.55	62.08	13.17	205.22
87.61	35.34	187.29	1.60	60.78	15.63	202.92
17.70	-74.34	19.22	10.48	54.34	174.49	193.71
25.57	-81.41	25.33	8.77	55.64	168.03	193.36
30.16	-87.05	27.54	8.19	56.04	164.55	192.10
28.68	-91.59	24.17	10.33	55.79	167.76	191.93
27.67	-86.05	25.50	9.44	55.71	165.29	190.80
17.44	-71.02	19.96	9.52	54.92	169.81	189.77
15.87	-72.03	17.66	11.30	54.44	171.66	189.32
25.92	-88.95	22.61	11.18	55.51	165.26	187.86

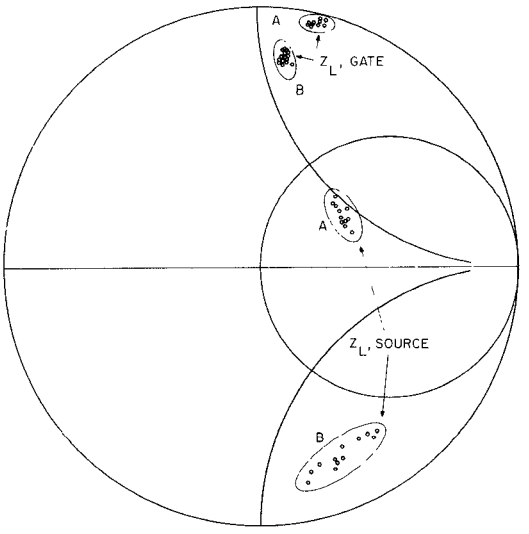

Fig. 4. Gate and source load impedance regions for maximum power at either port.

TABLE 2
Gate and source loading conditions for maximum source output power.

ReZs	ImZs	Ps(mW)	ReZg	ImZg	Pg(mW)	Ptot(mW)
74.74	43.52	265.99	0.46	63.53	3.24	269.24
77.31	43.24	241.37	0.73	63.42	5.16	246.53
73.11	47.63	237.75	0.30	64.98	1.78	239.52
81.97	42.79	203.22	1.27	63.44	9.15	212.37
35.56	38.80	192.12	1.55	62.09	13.15	205.27
35.63	38.77	192.04	1.55	62.08	13.17	205.22
37.51	35.34	137.29	1.60	60.78	15.63	202.92
90.30	37.13	165.29	1.97	61.92	16.99	182.28
91.64	33.48	163.44	1.95	60.64	19.35	182.79
95.24	46.84	163.29	1.75	64.92	10.63	173.92
90.91	40.14	155.12	2.17	63.17	16.11	171.24
93.56	32.29	130.27	2.75	61.61	24.51	154.77

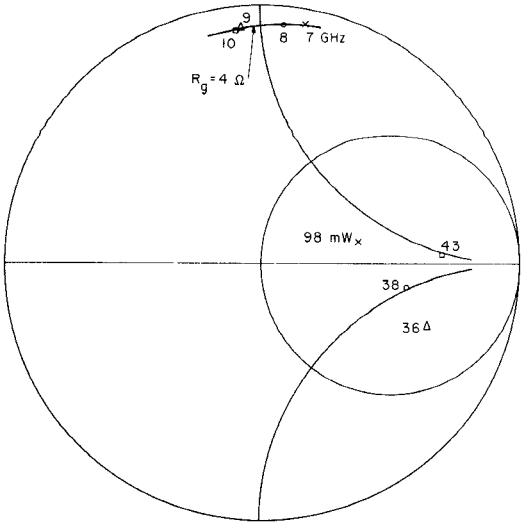

Fig. 5. Optimum source load, output power, and gate reactance versus frequency for a 4-ohm varactor resistance.

from the varactor tuning circuit at each frequency. It is evident that the power output falls quite rapidly with frequency. Given the source load impedance characteristics which approximate the optimum, the VCO performance can be predicted and the gate circuitry can be specified.

IV. SUMMARY

A large-signal measurement technique for characterizing the single frequency behavior of nonlinear active two-port networks has been presented. This technique can provide more useful and more complete design information for oscillators and amplifiers than other available methods. Application to common drain FET circuits had indicated optimal design criteria for single frequency and varactor-tuned oscillators.

V. ACKNOWLEDGEMENT

This work was supported by the Air Force Avionics Laboratory, Wright-Patterson Air Force Base, under contract F33615-77-C-1132.

REFERENCES

1. S. R. Mazumder and P. D. van der Puije, ""Two-Signal" Method of Measuring the Large-Signal S-Parameters of Transistors", IEEE Trans. Microwave Theory Tech., vol. MTT-26, pp. 417-420, June 1978.
2. D. E. Peck and D. F. Peterson, "A Measurement Method for Accurate Characterization and Modeling of MESFET Chips", IEEE-MTT-S Int. Microwave Symposium, Digest Technical Papers, June 1981, pp. 310-312.